extracting, from the circuit to be simulated, the plurality of partial circuits to inspect for equivalent operational characteristics;

inspecting the plurality of partial circuits to detect partial circuits exhibiting equivalent operational characteristics, based on the configurations of the plurality of partial circuits, and judging equivalence when the configurations of said plurality of partial circuits are mutually consistent; and

compressing the circuit by integrating the partial circuits exhibiting equivalent operational characteristics into one circuit and simulating the compressed circuit.

REMARKS

Claims 9-12, 14-24, 26-36, and 38-44 are pending in this application and have been rejected. Claim 9 has been amended without narrowing the claims within the meaning of <u>Festo Corp. v. Shoketsu Kinzoku Koygo Kabushiki Co.</u>, 56 USPQ2d 1865 (Fed. Cir. 2000). No new matter is being presented, and approval and entry are respectfully requested.

Entry of Amendment Under 37 C.F.R. §1.116

Applicant requests entry of this Rule § 116 Response for the following reasons: The amendment of claim 9 should not entail any further search by the Examiner because no new features are being added or no new issues are being raised, and the amendment does not significantly alter the scope of the claims and places the application at least into a better form for purposes of appeal. No new features or new issues are being raised.

The Manual of Patent Examining Procedures sets forth in Section 714.12 that "any amendment that would place the case either in condition for allowance or in better form for appeal may be entered." Moreover, Section 714.13 sets forth that "the Proposed Amendment should be given sufficient consideration to determine whether the claims are in condition for allowance and/or whether the issues on appeal are simplified." The Manual of Patent Examining Procedures further articulates that the reason for any non-entry should be explained expressly in the Advisory Action.

Objections to the Claims

In item 2 on page 2 of the Office Action, the Examiner objected to claim 9 for the reasons set forth therein. Applicant has amended claim 9 in this Response to change the word "existent" to "consistent," as suggested by the Examiner. Accordingly, Applicant respectfully requests withdrawal of the objection to claim 9.

Claim Rejections Under 35 U.S.C. §112, First Paragraph

In items 3-5 on pages 2-3 of the Office Action, the Examiner rejected claims 9-12, 14-24, 26-36, and 38-44 under 35 U.S.C. §112, first paragraph, for the reasons set forth therein, which are related to the terms "compressing" and "integrating." Applicant respectfully traverses this rejection for the reasons presented below.

In the present invention, a plurality of partial circuits exhibiting equivalent operational characteristics are integrated into one partial circuit. For example, Fig. 12 of the present invention, which is similar to Fig. 11, shows an example of a circuit having equivalent partial circuits. In Fig. 12, one partial circuit includes MOS transistors T40, T41, T44, T45, T48, and T49, and another partial circuit equivalent to the first partial circuit includes MOS transistors T42, T43, T46, T47, T50, and T51.

As can be seen by comparing Figs. 12 and 13, the two equivalent partial circuits have been integrated by removing all the circuit elements belonging to the second partial circuit between the input terminal and output terminal B. See pages 25 and 26 of the specification. Because the input terminal is common in these partial circuits, no special measures are required for the input terminals in the cancelled partial circuit. However, it is assumed that output terminal B in the cancelled partial circuit is connected to output terminal A in the remaining partial circuit, as shown in Fig. 13. See page 27 of the specification.

Thus, Pa in Fig. 13 corresponds to MOS transistors T40 and T42 in Fig. 12; Pb in Fig. 13 corresponds to MOS transistors T41 and T43 in Fig. 12; Pc in Fig. 13 corresponds to MOS transistors T44 and T46 in Fig. 12; Pd in Fig. 13 corresponds to MOS transistors T45 and T47 in Fig. 12; Pe in Fig. 13 corresponds to MOS transistors T48 and T50 in Fig. 12; and Pf in Fig. 13 corresponds to MOS transistors T49 and T51 in Fig. 12. Output terminal A in Fig. 12 corresponds to terminal G in Fig. 13. Output terminal B (terminal G' in Fig. 13) is virtually connected to terminal G, so that the output terminal B is handled as if it were terminal G. Thus,

the two equivalent partial circuits of Fig. 12 are integrated to form the circuit of Fig. 13. The circuit shown in Fig. 13 is referred to as a compressed equivalent circuit. See page 27 of the specification.

When the compressed circuit of Figure 13 is simulated, the input and output terminals are analyzed using circuit or current equations. At terminal C of Fig. 13, the current flowing from Pa is doubled because two partial circuits were integrated. The same analysis applies to terminal D.

Considering the output terminal in the compressed equivalent circuit, the current flowing from the output terminal of the compressed equivalent circuit can be calculated by assuming that only one output terminal of the equivalent partial circuits of Fig. 12 is connected to the compressed equivalent circuit. In other words, when current equations are considered for terminal G in Fig. 13, it can be assumed that only terminal G is connected to the compressed equivalent circuit. Conversely, when current equations are considered for terminal G' in Fig. 13, it can be assumed that only terminal G' is connected to the compressed equivalent circuit and that terminal G is not connected to the compressed equivalent circuit. In Fig. 13, it has been assumed that terminal G is connected to MOS transistors T62 and T63, and that terminal G and terminal G' are not connected to each other. See pages 4, 18, and 27 of the specification.

Accordingly, Applicant respectfully requests withdrawal of the rejection to the claims under §112, first paragraph.

Rejections Under 35 U.S.C. §112, Second Paragraph

In items 7-9 on page 3 of the Office Action, the Examiner rejected claims 15-18 under 35 U.S.C. §112, second paragraph, for the reasons set forth therein, which are related to the terms "intensity," "intensity of the influence," "frequency of shifting," "linking," and "based on the intensity." Applicant respectfully traverses these rejections for the reasons presented below.

The terms "intensity" and "intensity of the influence" refer to the intensity of the influence that operational characteristics of an external circuit have on operational characteristics of the compressed equivalent circuit. See pages 21, 23, 25, and 26 of the specification.

The following background information is provided to understand the influence of the operational characteristics of an external circuit. In general, a circuit having a plurality of MOS transistors operates by controlling the current flowing through the source terminal and the drain

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terminal of the MOS transistors in response to the change in an input signal supplied to the gate terminal of the MOS transistors. Each source terminal of a MOS transistor is electrically isolated from the gate terminal by an oxide film. Each drain terminal of a MOS transistor is also electrically isolated from the gate terminal by the oxide film. However, a first capacitance exists between the source terminal and the gate terminal of the MOS transistor and a second capacitance exists between the drain terminal and the gate terminal. A first displacement current is generated due to the first capacitance, and a second displacement current is generated due to the second capacitance.

The thickness of the oxide film decreases as micro-fabrication techniques improve. If the thickness of the oxide film decreases, both the first capacitance and the second capacitance increase. Therefore, neither the first displacement current nor the second displacement current is negligible. Also, if the thickness of the oxide film decreases, neither the first leakage current flowing through the source terminal and the gate terminal nor the second leakage current flowing through the drain terminal and the gate terminal is negligible.

The displacement and leakage currents cause the voltage in the source terminal and the voltage in the drain terminal to fluctuate. Consequently, the voltage in the gate terminal also fluctuates and operational characteristics of the gate terminal vary with fluctuation in the voltage in the gate terminal. The voltage in the source terminal and the voltage in the drain terminal fluctuate in opposite directions to the voltage in the gate terminal. Therefore, operational characteristics of the gate terminal vary so that the phase of the voltage applied to the gate terminal lags.

Considering Fig. 8 of the present invention, if the intensity of the influence output terminal E has on output terminal G is defined as S_1, the intensity of the influence output terminal C has on output terminal G is defined as S_2, and the intensity of the influence output terminal A has on output terminal G is defined as S_3, then $S_1 > S_2$ and $S_2 > S_3$.

If an external terminal B' is connected to a given terminal A' via a resistor or a channel of a transistor, DC current flows through the external terminal and the given terminal. Therefore, operational characteristics of the given terminal are substantially the same as those of the external terminal, except that the phase of the voltage in the terminal differs from that of the voltage in the external terminal. In this case, the intensity of the influence the external terminal has on the given terminal is relatively large.

In contrast, if the external terminal B' is connected to a given terminal A' via a gate terminal of at least one MOS transistor, the external terminal has only a small influence on the given terminal through the capacitance between the source terminal and the gate terminal, the capacitance between the drain terminal and the gate terminal, the small leakage current flowing through the source terminal and the gate terminal, and the small leakage current flowing through the drain terminal and the gate terminal. In this case, the intensity of the influence the external terminal has on the given terminal is weakened.

The term "frequency of shifting" is used for assessing the intensity of the influence an external terminal on the output side of a given terminal has on the given terminal. The number of MOS transistors encountered or the number of gate terminals that exist, when tracing an arbitrary path "linking" the external terminal to the given terminal is defined as the "frequency of shifting" of the external terminal with respect to the given terminal.

In the example shown in Fig. 8 of the present invention, two paths link external terminal A to a given terminal E. One of the two paths links terminal A to transistor Tb to terminal C to transistor Th to terminal E. Two gate terminals of a MOS transistor exist in the path. Thus, the "frequency of shifting" of the external terminal A with respect to the given terminal E is 2. Similarly, the "frequency of shifting" of external terminal A with respect to a given terminal C is 1, and the "frequency of shifting" of external terminal A with respect to a given terminal G is 3.

The phrase "based on the intensity" is used when determining whether a plurality of partial circuits are equivalent circuits by appropriately defining the "frequency of shifting" as the lower limit of the "intensity of the influence". See pages 21, 23, 25, and 26 of the specification.

When determining equivalence of the partial circuits with relatively high accuracy, the influence that an arbitrary output circuit, having a predetermined fan out, has on each of the partial circuits must be negligible. Thus, the "frequency of shifting" is set to a predetermined value, preferably set to the value of 2, as the lower limit of the "intensity of the influence." If the intensities of influence of an external terminal of the partial circuits are greater than or equal to the predetermined value, then the partial circuits are considered to be equivalent (i.e., "quasi-equivalent"). The "frequency of shifting" may be set to other values. For example, if it is necessary to carry out circuit simulations at relatively high speed, even if accuracy of the inspection for equivalence of partial circuits somewhat deteriorates, then the "frequency of shifting" may be set to a value of 1 as a lower limit on the "intensity of the influence."

For example, referring to Fig. 12, two partial circuits 33 and 34 are inspected for equivalence. The two partial circuits 33 and 34 are not equivalent because the output terminals

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of the partial circuits are connected to different transistors T58 and T59. The intensity of the influence of MOS transistors T58 and T59 on terminals A and B is set at the value of 2. The frequency of shifting from MOS transistor T58 to terminal A is 2. Thus, the intensity of influence on terminal A is 2. The frequency of shifting from MOS transistor T59 to terminal B is also 2. Thus, the intensity of influence on terminal B is 2. Because the intensities of the influence of the MOS transistors T58 and T59 on terminals A and B are 2, which is greater than or equal to the predetermined value of 2, the two partial circuits 33 and 34 are considered as being quasi-equivalent circuits.

Accordingly, Applicant respectfully requests withdrawal of the rejection to the claims under §112, second paragraph.

Rejections Under 35 U.S.C. §§ 102 and 103

On pages 4-8 of the Office Action, the Examiner rejected claims 9-12, 14-24, 26-36, and 38-44 under 35 U.S.C. §102(b) as being anticipated by Filseth (U.S. Patent No. 5,473,546); or Yokomizo et al. ("A New Circuit Recognition and Reduction Method for Pattern Based Circuit Simulation," IEEE Custom Integrated Cir. Conf., pp. 9.4/1-9.4/4); or Chakrabarti et al. ("An Improved Hierarchical Test Generation Technique for Combinational Circuits with Repetitive Sub-Circuits," IEEE Proc. Test Symp., pp. 237-243).

On page 8 of the Office Action, the Examiner rejected claims 9-12, 14-24, 26-36, and 38-44 under 35 U.S.C. §102(e) as being anticipated by Hachiya (U.S. Patent No. 6,031,979).

On pages 9-11, the Examiner rejected claims 9-12, 14-24, 26-36, and 38-44 under 35 U.S.C. §103(a) as being unpatentable over Shinsha et al. (U.S. Patent No. 4,882,690); or Wang et al. ("Restructuring Binary Decision Diagrams Based on Functional Equivalence," IEEE Design Automation, pp. 261-65); or Kuehlmann et al. ("Equivalence Checking Using Cuts and Heaps," IEEE Proc. 1997 Design Auto. Conf., pp. 263-68).

The Examiner has either repeated or modified his prior art rejections from the prior Office Action. Applicants maintain their arguments with respect to these claims, as found in the previously filed responses.

CONCLUSION

It is submitted that none of the references, either taken alone or in combination, teach the present claimed invention. Thus, claims 9-12, 14-24, 26-36, and 38-44 are deemed to be in a condition suitable for allowance. Reconsideration of the claims and an early Notice of Allowance are earnestly solicited.

If there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

Finally, if there are any additional fees associated with filing of this Response, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please **AMEND** the following claim:

9. (THREE TIMES AMENDED)   A method of carrying out simulation of a circuit, comprising:

inputting data comprising configurations for a plurality of partial circuits, and connectional relationships for input and output terminals of the partial circuits;

extracting, from the circuit to be simulated, the plurality of partial circuits to inspect for equivalent operational characteristics;

inspecting the plurality of partial circuits to detect partial circuits exhibiting equivalent operational characteristics, based on the configurations of the plurality of partial circuits, and judging equivalence when the configurations of said plurality of partial circuits are mutually [existent] consistent; and

compressing the circuit by integrating the partial circuits exhibiting equivalent operational characteristics into one circuit and simulating the compressed circuit.